REMARKS

In the Office Action the Examiner rejected claims 3 and 5 under 35 U.S.C. 112, second paragraph, for being indefinite, rejected to claims 1-6 and 8-15 under 35 U.S.C. 102 as being anticipated, rejected claims, and objected to claim 10 for an informality. Claims 1, 4, 6, and 8-15 remain under examination.

With regard to the objection to claim 10, claim 10 has been amended consistent with the manner suggested by the Examiner.

With regard to the rejection of claims 3 and 5, the Examiner viewed these claims as not correctly describing the operation of the clocked inverters in that when they are disabled, they do not perform an inversion. In light of the inputs of both of the clocked inverters being held to a logic high when the clocked inverters are being disabled, applicants believe the Examiner's view of the operation is correct. Claims 3 and 5 attempted to point out that only the inversion of one input logic state needed to be disabled. Disabling the clocked inverter for the other logic state was unnecessary because the other logic state would not occur so no circuitry was needed for that case. This is a benefit of applicants' approach, but perhaps claims 3 and 5 do not convey the intent. Accordingly, claims 3 and 5 have been canceled.

The rejection for anticipation was mostly based on Weibernеit, but the Examiner also applied Lin to claim 1. Both Wiebernet and Lin are deficient because neither meet the requirement of claim 1 of "providing both the first and second input signals at a predetermined one of the complementary logic states during the second clock state." In the case of Weibernеit, the input signals are always complementary. For example, applicants have not been able to find that inverter S1 is ever disabled. With regard to Lin, the signals are either complementary or indeterminate. In addition to the benefit pointed out above with respect to having both signals in a predetermined state of needing only to disable the inverters for that logic state, another benefit is precharging the inputs and outputs of the clocked inverters to the logic high state, which is the faster state to transition out of. A logic high to logic low transition is faster, for a given transistor size, because it is achieved with N channel transistors. Although a logic low to logic high transition is possible using an N channel transistor, there are issues concerning the threshold voltage drop across the N channel transistor that require increased complexities such as a parallel P channel transistor or bootstrapping or by compensating for the logic high not achieving the full VDD level. Accordingly, applicants submit that claim 1 is patentably distinct over Wieberneit

and Lin. Claim 10 has been amended to have a similar limitation to that distinguished from Weiberneit and Lin. In light of the above, applicants submit that a different analysis applies to the dependent claims.

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicant, Applicant refuses to subscribe to any of these statements, unless expressly indicated by Applicant.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

Respectfully submitted,

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